Design of a Low-power Ultrasound Transceiver for Underwater Sensor Networks

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***Abstract*—This paper presents an ultrasound (US) transceiver including a transmitter and a receiver for underwater wireless sensor nodes, where low-power operation is desired to extend the life-time of the network. A system-level analysis of the underwater communication has been performed by taking into account the underwater propagation and the medium characteristics to show their impact on the overall performance. In addition, a low-noise amplifier using an inverter-based topology has been introduced to ensure power efficiency of the receiver, where a bulk-feedback method is proposed to stabilize the output bias point of the inverter. Simulation results show that the proposed transceiver has a scalable power consumption from 1.95μW to 10.4μW while achieving 100μV to 20μV sensitivity at a 10^{-3} BER level.**

I. Introduction

Underwater wireless sensor networks (UWSNs) are useful for various emerging applications such as environmental monitoring, early detection of disasters, and localization in pipes [1]. A low-power transceiver is required in these applications to achieve sufficiently long life-time of the network since the sensor nodes are required to operate continuously. US signals are commonly preferred over RF signals for the data exchange among sensor nodes because of their relatively low attenuation in underwater conditions [2]. On the other hand, US data-rate is limited due to the low speed of US signals, and the communication bandwidth is bounded by that of the transducer, which is much lower compared to terrestrial RF applications [3]. The limited bandwidth of the transducer limits the choice of the communication schemes to low-complexity amplitude or frequency modulation methods, which can be sensitive to e.g. multi-path propagation and interference in the communication among different sensor nodes. In this work, a design procedure for a low-power US Transmitter and US Receiver for UWSNs will be described. In order to determine the power trade-off between transmitting and receiving the US data, a system level analysis will be performed, where a top-down approach is used to capture the effects of the transducer and the underwater medium as well as the circuit parameters. The proposed US transceiver is shown in Fig.1. An on-off keying (OOK) scheme has been chosen for the communication due to its simplicity and low power operation [4]. The receiver comprises a low-noise amplifier (LNA), a variable gain amplifier (VGA), an envelope-detector (ED), a low pass filter (LPF), and a comparator to reconstruct the incoming data. To minimize power consumption of the amplifiers, an inverter-based topology has been used, where a bulk feedback method is proposed to stabilize the output bias point of the inverter. On the transmitter side, a power-efficient two-stage class-D buffer has been used thanks to relaxed linearity constraints of the OOK scheme. The paper is organized as follows: In Section II, the system-level analysis of the US transceiver for underwater communication is performed. The details of the circuit design are presented in Section III. Post-layout simulation results are given in Section IV. The performance of the US transceiver with respect to system-level analysis is discussed in Section V. Finally, Section VI concludes this study.

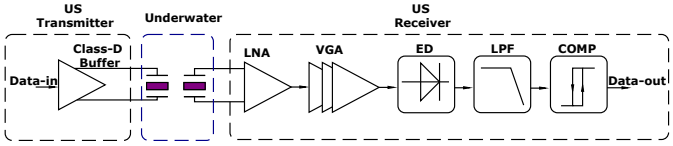

Figure 1. The proposed architecture of the US transceiver. The transducer has a band-pass transfer centered around its resonance frequency.

II. System Level Analysis of the Underwater Communication

Piezoelectric transducers are considered in this work as they do not require external bias [3]. These transducers can be simply modelled by their parallel capacitance, C_p, in transmitting mode [5]. As a result, the dominant power is spent by the transmitter circuit to charge and discharge C_p. Furthermore, since an OOK based scheme is chosen, linearity is not a relevant factor. Thus, it is possible to use a class-D output buffer [3]. As a result, the power consumption of the transmitter, P_{Tx}, can be calculated as

$$P_{Tx} = \frac{C_p \cdot V_{drive}^2 \cdot f}{\alpha}, \qquad \text{[W]} \tag{1}$$

where V_{drive} is the amplitude of the driving signal, f is the data rate, α is the efficiency of the buffer. Assuming a single omni-directional transducer working in its linear regime, the applied voltage, V_{drive}, will generate a source level pressure, SL, which can be found as

$$SL = S_v + 20\log(V_{drive}), \qquad \text{[dB } re\,\mu\text{Pa]} \tag{2}$$

where S_v is the transmit sensitivity of the transducer. The passive sonar equations [2], [6] can be used to estimate the pressure level at the receiver. In this case, the received

sound pressure level, SPL, can be calculated as

$$SPL = SL - TL, \qquad [\text{dB } re\,\mu\text{Pa}] \tag{3}$$

where TL is the transmission loss of the environment. The corresponding received voltage level, V_{rec}, is given by

$$SPL = |S_r| + 20\log(V_{rec}), \qquad [\text{dB } re\,\mu\text{Pa}] \tag{4}$$

where $|S_r|$ is the receive sensitivity of the transducer. As a result, the relationship between V_{drive} and V_{rec} can be obtained by substituting equations (3) and (4) into (2) to write

$$\begin{aligned} V_{drive} &= V_{rec} \cdot 10^{\frac{|S_r| - S_v + TL}{20}} \\ V_{drive} &= V_{rec} \cdot K, \qquad [\text{V}] \end{aligned} \tag{5}$$

where the constant K captures the combined effects of the transducer, the communication frequency and distance, and the medium of interest. The level of V_{rec} is important for the estimation of the power consumption of the receiver, since it determines the signal-to-noise ratio (SNR). Moreover, assuming that the VGA provides sufficiently large gain to suppress the noise and non-linearity of the ED, the noise factor of the LNA basically determines the input noise level of the front-end, which makes its power consumption dominant in the receiver chain. To estimate the power consumption of the LNA, the noise-efficiency factor (NEF) of an amplifier can be used. It is defined as

$$NEF = V_{in,noise}\sqrt{\frac{2I_{amp}}{\pi \cdot U_t \cdot 4kT \cdot BW}}, \tag{6}$$

where $V_{in,noise}$ is the total input-referred rms noise voltage, U_t is the thermal voltage, k is the Boltzmann constant, T the temperature, I_{amp} and BW are the current consumption and the bandwidth of the LNA. The ratio between V_{rec} and $V_{in,noise}$ needs to be larger than 12dB to have 10^{-3} bit error rate in OOK [4], and BW can be assumed to be equal to the transducer bandwidth. Therefore, given that NEF of 2 is achievable with inverter-based LNA topologies [7], I_{amp} and thus the power consumption of the LNA can be calculated. Fig.2 shows the estimated amount of power consumption in the transmitter and the LNA with respect to the amplitude of the received voltage, assuming a commercial transducer [8] is used in a shallow water[1]. Further assumptions are: 80% efficiency of the transmitter, C_p of 1nF, the communication distance is $10m$, the bandwidth is $50kHz$, the data rate is $250bps$, and the supply voltage of the LNA is $0.6V$. As a result, the power of the LNA dominates when a higher sensitivity must be achieved, whereas the transmitter power dominates when sensitivity is relaxed. It should be noted that in this discussion no duty-cycling is considered. The methodology described in this section indicates that there is an optimum power consumption for the underwater US transceiver when the performance of the receiver and the transmitter are considered together, rather than focusing on the performance of the individual blocks.

[1]For a communication distance of $10m$ and a frequency of $200kHz$, the value of TL in shallow water is calculated to be 30dB at 27 °C temperature [2], and around $20dB$ margin is added to TL to account for the additional losses and the variation of the underwater medium [6].

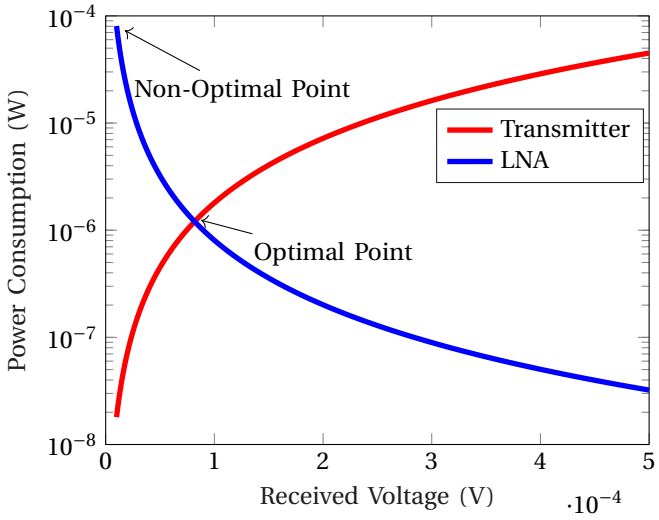

Figure 2. Power consumption behaviour of Transmitter and LNA

III. Circuit Design

A. Low Noise Amplifier and Variable Gain Amplifier

A voltage amplifier with high input resistance is desired for the piezo transducers due to their relatively low impedance at the resonance frequency [5]. A closed-loop capacitor feedback architecture as shown in Fig.3 is selected for the LNA. An inverter-based topology is chosen for the core amplifier to increase the transconductance and improve the NEF. No current sources in series with the

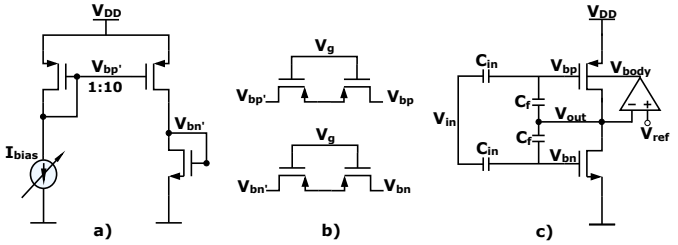

Figure 3. Circuit implementation of the LNA a) Biasing current mirror b) Pseudo-Resistors c) Capacitive-feedback amplifier with bulk-feedback.

inverter are used to bias it. This makes possible to lower aggressively the supply voltage, V_{DD}. The inverter transistors are biased in weak inversion and use relatively large aspect ratio to maximize the current efficiency. To reduce the effects of parasitic capacitors on the in-band gain, the capacitor splitting method [9] is applied and the transistors are biased separately. The bias current, I_{bias}, is multiplied 10 times by the the current mirror. The gate voltages for the input transistors (V_{bp} and V_{bn}) are provided through pseudo-resistors (PRs) having a large resistance (100MΩ to 10GΩ) to set the high-pass corner below 1kHz. The gate voltage (V_g) of the PRs is provided separately to control their resistance against process variations. An important point in the inverter-based topology is to stabilize the output bias point against process variations and mismatches in the biasing networks. This can be achieved by applying a

negative feedback to control the pull-up current provided by a transistor in series with the inverter [7], or to control the gate bias of one of the transistors in the inverter [9]. The former option limits the minimum V_{DD} level, whereas the latter results in extra parasitic capacitance to the gate of one of the input transistors, which degrades the gain and the noise performance. Although this problem can be solved via a dynamic bias loop [9], this technique is not applicable to continuous operations since it requires a pre-determined on and off time of the LNA. To solve this problem, a bulk-feedback method is proposed, where the negative feedback is applied to the bulk terminal of the p-type transistor to control its threshold voltage via the body-effect. The output DC point is compared to a mid-rail reference voltage (V_{ref}) and the error signal is fed back to the bulk terminal by an error amplifier (EA), thereby avoiding parasitic loading on the gate of the input transistors. On the other hand, this method requires higher EA gain compared to the method in [9] due to reduced bulk transconductance, and the EA output voltage should be around V_{DD}. As a result, a supply voltage (V_{DDH}) higher than V_{DD} is used for the EA, which is built as a conventional folded-cascode amplifier with diode-connected load [10]. The power overhead is negligible since the bias current of the EA is kept to $10nA$ to slow down its operation. A similar topology is used for the amplifiers of the VGA; here five inverter-based stages like the one depicted in Fig.3 are cascaded to provide high gain, as shown in Fig.4. A reduced closed-loop gain with respect

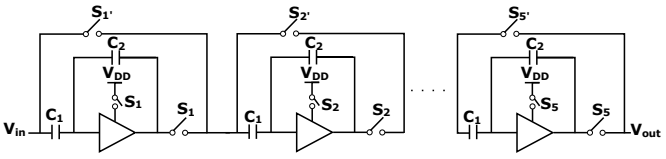

Figure 4. Schematic diagram of the VGA.

to the LNA as well as reduced bias current is used for the VGA stages since these amplifiers are not noise-limited. By appropriately selecting the switches (S_1 to S_5), the number of cascaded stages, and thus the total gain can be changed.

B. Envelope Detector, Low Pass Filter, and Comparator

The amplitude of the modulated signal can be extracted by using the ED, where a common drain topology [11] has been chosen as shown in Fig.5a. The transistor is biased in weak-inversion to provide the non-linearity. A $5pF$ capacitance C_L is used as hold capacitor. The ED is followed by the LPF given in Fig.5b, which is implemented as a $Gm-C$ filter for low-power operation. A simple inverter is used as a transconductance block. After the signal is squared and filtered, a hysteresis comparator as shown in Fig.5c has been used to compare the amplitude with an external reference (V_{ref2}) and obtain a digital output signal.

C. Transmitter

As discussed in section II, a class-D buffer as shown in Fig.6 is used as a transmitter. It is formed by a chain of inverters sized to drive large capacitance load of 1nF. In this circuit a level shifter and inverters using 3.3.V transistors

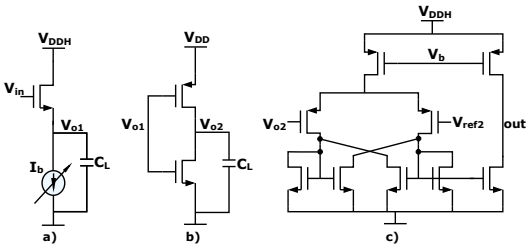

Figure 5. The schematic of the a) ED b) LPF c) Comparator (The biasing network of the circuits are not shown for simplicity)

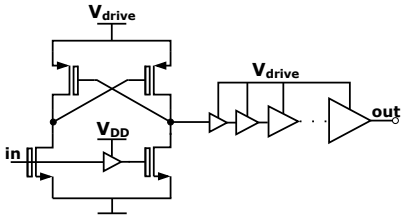

Figure 6. The schematic of the Transmitter

have been used, to enable to use a separate supply level, V_{drive}, higher than the one used in the receiver.

IV. Simulation Results

A 65nm commercial CMOS technology is used for the implementation. The I_{bias} of the LNA is provided from outside of the chip, and can be tuned to achieve various power and noise performances, as summarized in Table I. V_{DD} can be lowered down to 0.4V for low-power operation. The current drawn from the V_{DD} (including LNA bias and core amplifier), I_{total}, varies from $0.33\mu A$ to $7.1\mu A$ and corresponds to a total power consumption of $0.2\mu W$ to $4.26\mu W$. The functionality of the bulk-feedback method is shown by the output DC voltage, $V_{dc,out}$, which is set to half of the V_{DD} (V_{ref}) with a maximum error of $4mV$. The capacitance ratio, $\frac{C_{in}}{C_f}$, is set to 10. The simulated closed-loop gain (A_v) is 19dB in all cases. Since large aspect ratios are utilized in the inverter, the 1dB discrepancy in the closed-loop gain is due to the parasitic capacitors at the inverter input. A 0.6V supply is used for the VGA, where the capacitance ratio is set to achieve $12dB$ closed loop gain of each stage. The maximum power consumption of the VGA is $1.1\mu W$ when the five stages are all activated, and it can be reduced down to $0.45\mu W$, depending on the input signal level. A 1.2V supply voltage is used for the EA, ED, and the comparator where the power consumption of these circuits at their typical biasing conditions is $0.012\mu W$, $0.036\mu W$, and $0.038\mu W$, respectively. Total power consumption of the US receiver is scalable from $1\mu W$ to $7\mu W$, while achieving an input-referred noise density ($IRND$) from $28.4nV/\sqrt{\text{Hz}}$ to $8.5nV/\sqrt{\text{Hz}}$ at $200kHz$ and a sensitivity from $100\mu V$ to $20\mu V$. On the transmitter side, the maximum available voltage in the technology used is 3.3V, which results in a power consumption of $3.4\mu W$ for the 1nF transducer considered in this work. This can be lowered down to

Table I. PERFORMANCE OF THE LNA

V_{DD} (V)	I_{bias} (nA)	I_{total} (μA)	$V_{dc,out}$ (mV)	A_v (dB)	IRND@200kHz $(nV/\sqrt{Hz})$
0.6	10	0.33	299	19	26.2
	100	3.69	299	19	10.2
	200	7.1	299	19	8.5
0.4	10	0.41	198	19	28.4
	100	2.68	196	19	11.4

$0.45\mu W$ and $1\mu W$ when V_{drive} is set to 1.2V and 1.8V, respectively.

V. DISCUSSION

The power consumption for the total US transceiver, including transmitter and receiver, with respect to the received voltage level, is shown in Fig.2. This trend shows an optimum where the power used in the transmitter and receiver are similar. When a more challenging scenario is to desired, e.g. when a longer communication distance is needed in harsh environmental conditions, the optimal point moves to higher power levels. This problem is addressed in this work, and a flexible transceiver is proposed to cover a range of performance, as summarized in the bottom of Table II. The flexibility is achieved by varying V_{drive} at the transmitter and I_{bias} at the receiver. As a result, considering the 10m underwater communication scenario described in Sec.II, it can be shown that a voltage sensitivity around $70\mu V$ leads to an optimum power consumption of $2.20\mu W$, which is achievable with the proposed transceiver when $V_{drive} = 1.8V$, and $I_{bias} = 10nA$.

The performance of the proposed US transceiver and its comparison with relevant integrated US transceivers from recent literature is given in Table II. Each work uses the same modulation scheme and data-rate, but the prior art focuses on transmission in air, while we exploit US for underwater communication, where the US signal attenuation is much smaller. A super-regenerative receiver is proposed in [12], where a supply voltage of 0.3V is used and a power consumption of $1\mu W$ on the receiver side is achieved for $20\mu V$ sensitivity. The work in [4] achieves a $4.4\mu W$ receiver power consumption for $20\mu V$ sensitivity. Our work relaxes the receiver sensitivity requirements thanks to the underwater environment. To reach 10m communication distance, only $70\mu V$ receiver sensitivity is needed, which brings the power consumption in our receiver down to $1.2\mu W$. Besides, exploiting an holistic optimization of both transmitter and receiver power for the low-loss underwater environment, we achieve a total power consumption for the 10m communication link of only $2.2\mu W$.

VI. CONCLUSION

The underwater medium offers various emerging applications demanding low-power circuit design to enable long-term continuous operations of the sensor nodes. This work presents a system-level design approach of a US transceiver, where it is shown that the minimum power consumption can be achieved when transmitter and receiver performance are optimized together. The circuit implementation of the overall transceiver is described, and post-layout simulations show the suitability of the proposed circuits for use in underwater wireless sensor networks achieving extremely competitive, μW power budgets for communication in the 10m distance range.

Table II. PERFORMANCE COMPARISON OF THE PROPOSED US TRANSCEIVER

Specs	[4]	[12]	This Work*	
Frequency (kHz)	40.6	41	200	
CMOS process (nm)	65	250	65	
Modulation	OOK	OOK	OOK	
Data Rate (bps)	250	250	250	
Supply Voltage (V)	0.6	0.3	1.2 - 0.6 - 0.4	
Off-chip L&C	Yes	Yes	No	
On-CHIP Rx&Tx	No	No	Yes	
Communication Distance (m)	8.6 (air)	6.3 (air)	10 (shallow underwater)	
			Range	Optimal
Tx Power Consumption (μW)	16000	1000	0.45 - 3.4	1
Rx Power Consumption (μW)	4.4	1	0.95 - 7	1.2
Sensitivity (μV)	20	20	100 - 20	70

*Based on post-layout simulations

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