A 0.1nW-1µW All-dynamic Capacitance-to-Digital Converter with Power/Speed/Capacitance Scalability

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***Abstract*— A versatile, low power and energy efficient Capacitance-to-Digital Converter (CDC) for Internet-of-Things (IoT) is presented, based on an all-dynamic architecture with adaptable speed, resolution and range. Sampling rates from 1S/s up to 100kS/s are supported and capacitances from 1.23 to 24.59pF can be digitized while the power scales inherently from 0.1nW to 1µW. This makes the design versatile to efficiently deal with a variety of sensors with different speed requirements and different capacitance values. The 0.1nW lowest absolute power is >20x smaller than prior-art, and the Figure-of-Merit (FoM) from 18 to 59fJ/conv-step is also the lowest among prior designs. As example, by connecting a MEMS pressure sensor, this chip can measure environmental pressure with only 0.8nW at a speed of 100S/s.**

***Keywords*— CDC, SAR ADC, dynamic, versatile, IoT**

I. Introduction

Recent IoT applications require ultra-low power on demand sensing circuits due to the scarce energy available. Capacitive sensors are well suited for low power sensing as they consume only dynamic power, and they can be used to measure parameters such as pressure, acceleration, and humidity. In order to save power and to reduce physical size, capacitive MEMS sensors tend to have a relatively small capacitance (e.g. 2-3pF for an exemplary accelerometer, 8-12pF for a pressure sensor). On top of this, different sensor types or applications require a different speed. For example, an environmental pressure sensor only needs a relatively low rate, while an accelerometer measuring movements will require a much higher rate. Therefore, a low-power CDC with an efficiently adaptable speed and an efficiently adaptable range from 1 to 30pF is critical to cover different sensors and applications.

SAR-based CDCs can achieve a very good power efficiency down to 35fJ/conv-step [1][2], but their absolute power is in µW-range. Recent low power designs [3][4] can achieve a low absolute power of 110-160nW, at the expense of decreased power efficiency. On top of this, these designs show a limited speed scalability. In [5], the speed can scale by about 13x, but the power scales only about 2.6x. The quasi-dynamic architecture in [1] achieves about 4x power and speed scalability. In [6], a minimum power of 2.8nW is achieved while speed and power can be scaled by >3000x with a power efficiency of 290fJ/conv-step.

To combine a low absolute power with high versatility and state-of-the-art efficiency, a versatile CDC based on an all-dynamic architecture is proposed, which consists of a passive single-armed capacitive bridge and an asynchronous SAR ADC. Thanks to this all-dynamic architecture, the power inherently scales with the speed over 4 orders of magnitude. By using an array of on chip reference capacitors, this design is able to cover an input range of 1.23~24.59pF. Besides, it can deal with both single-ended and differential capacitive sensors. The leakage power is optimized to 0.1nW, such that the efficiency is maintained even for very low sample rates.

This paper is organized as follows: the versatile CDC is introduced in Section II, measurement results are presented in Section III, and conclusions are drawn in Section IV.

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II. Proposed All-Dynamic Versatile CDC

A. Architecture

The architecture of the versatile CDC is shown in Fig. 1. It includes a single-armed capacitive bridge, which is essentially a capacitive voltage divider, and a differential 10b asynchronous SAR ADC. Both blocks only use dynamic circuits, hence consuming only dynamic power. A single-armed capacitive bridge was also used in [4] with an integrating amplifier for charge transfer, while only passive charge sharing circuits are used in this design. A single-ended sensor C_s can be connected externally. To deal with different nominal C_s values, the on-chip reference C_r can be programmed by Cr_sel<2:0> in a range from 2.5pF to 17.5pF with a step of 2.5pF. Complementary switches are used to connect both sides of the bridge to VDD or VSS with the help of CLK1 and CLK2, producing a regular or reversed output V_c. The reset switches in the capacitive bridge are controlled by clock signal RST, and they are used to reset C_r and C_s when required. As indicated in Fig. 1, the capacitive bridge is also able to deal with differential sensors (C_{d1} and C_{d2}), for instance for a capacitive accelerometer. In this case, C_r is disabled, the top and bottom sides of the differential sensor are directly connected to the bridge switches, and the middle point of the differential sensor is directly connected to the ADC. The SAR ADC samples V_c with clock SCLKP and the reversed V_c with clock SCLKN on

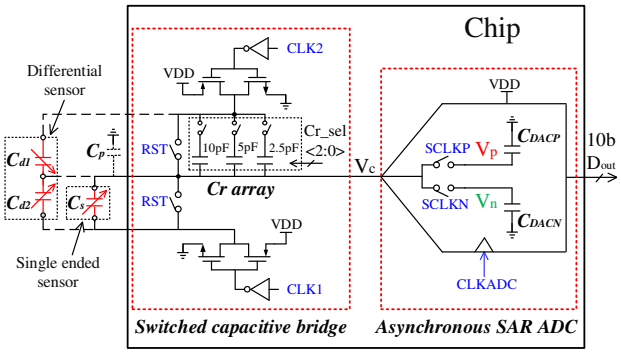

Fig. 1. Architecture of the versatile Capacitance-to-Digital Converter.

C_{DACP} and C_{DACN} separately, and performs the digitization at the rising edge of CLKADC. Both the capacitive bridge and the SAR ADC use a 0.6V supply to save power and to achieve a ratiometric measurement. The clock drivers use a 0.8V supply to provide enough switch linearity and to reduce bridge leakage power.

B. *Circuit operation*

The operation of the sensor interface is very similar when dealing with single-ended and differential sensors. Thus, the operation and calculation will be explained only for a single-ended sensor. The waveforms in Fig. 2 explain the operation over time. The reset phase comes first: CLK1 and CLK2 are low, so both the top and bottom side of the bridge are connected to ground. RST, SCLKP and SCLKN are high, thus resetting nodes V_c, V_p, and V_n to ground. Then, the first sampling phase starts. At this period CLK1 is high while CLK2 remains low, thus connecting the top/bottom side of the bridge to VSS/VDD respectively. SCLKP is also high to connect the bridge output to the positive side of the ADC's DAC (C_{DACP}). This voltage V_p can be calculated as:

$$V_p = VDD \cdot C_s / (C_s + C_r + C_{DACP} + C_p) \quad (1)$$

where C_p is the parasitic capacitance, which is relatively small compared to C_s. After V_p is sampled, CLK1 goes low, and RST goes high again to reset the bridge for the preparation of the second sampling phase. In the second sampling phase, CLK2 goes high while CLK1 remains low, and SCLKN is high to sample the reversed bridge output on C_{DACN}. This voltage V_n can be calculated as:

$$V_n = VDD \cdot C_r / (C_s + C_r + C_{DACN} + C_p) \quad (2)$$

In this way, a full bridge measurement is obtained with only a single arm, as the differential voltage $V_p - V_n$ is given by:

$$V_p - V_n = VDD \cdot (C_s - C_r) / (C_s + C_r + C_{DAC} + C_p) \quad (3)$$

where $C_{DAC} = C_{DACP} = C_{DACN}$. The ADC digitizes this differential signal, the output code D_{out1} is produced after the conversion delay, and then all circuits power down automatically thanks to their dynamic nature. As (3) shows, the sampled voltage is non-linear with the sensed value C_s. However, this non-linearity is entirely predictable by equation (3) and therefore can be compensated afterwards. Moreover, most sensors show intrinsic non-linearity that needs to be calibrated, thus these calibrations can be done simultaneously.

Because V_p is sampled before V_n, V_p may have more signal droop due to sampling switch leakage. Even though the entire sampling is finished within 3µs, this can still lead to slight inaccuracy. To solve this problem and to cancel ADC offset, an optional "double sided" measurement (similar to [7]) can be implemented after the first "single sided" measurement is done. In this case, CLK2 goes high first when sampling on C_{DACP}, while CLK1 goes high afterwards when sampling on C_{DACN}. By doing this, a reversed version of the differential voltage is sampled by the ADC, which produces a reversed digital output D_{out2}. By subtracting D_{out2} from D_{out1}, the double sided

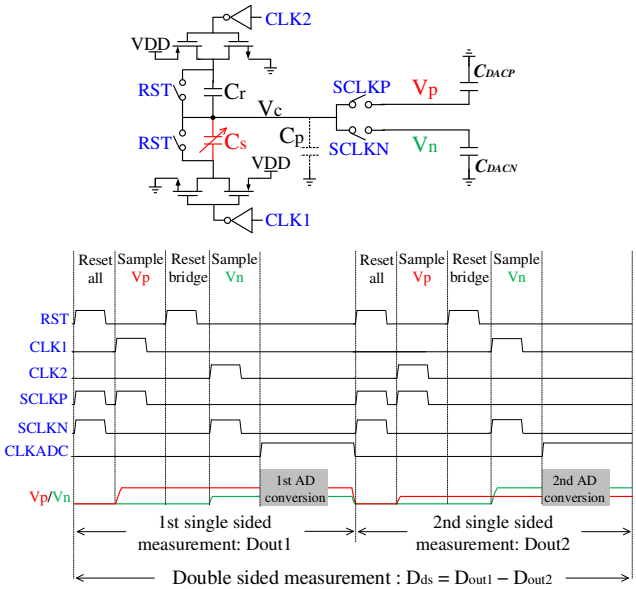

Fig. 2. Core of bridge and ADC (top) and operation waveforms (bottom).

measurement D_{ds} is obtained, which is able to compensate the aforementioned errors and to improve SNR by 3dB [7].

C. *SAR ADC with adaptable sensitivity*

An asynchronous 10b SAR ADC [8] is used such that a single clock edge enables the entire ADC operation. The DAC capacitance is only 300fF with 250aF unit capacitors to save power while achieving sufficiently low kT/C noise. C_{DAC} is sufficiently small compared to C_s and C_r, so that passive charge sharing between bridge and ADC is possible without causing prohibitive signal attenuation. Considering that C_s typically varies within a small range around the nominal value, only a small part of the ADC's signal range would be used. Therefore, two attenuation capacitors (300/600fF) are added to the DAC (Fig. 3 top) to reduce the effective ADC input range while increasing the ADC sensitivity. Using Sens_sel<1:0>, the ADC sensitivity can be increased up to 4x (Fig. 3 bottom). High-Vth transistors with increased length are used for the ADC logic to minimize leakage power. The sampling switches are

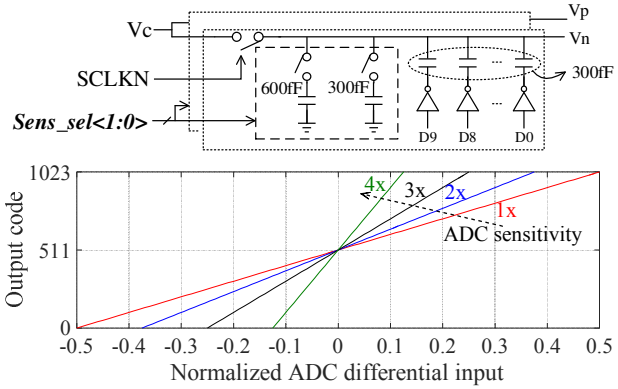

Fig. 3. Configurability of the ADC sensitivity.

implemented with CMOS gates rather than using dynamic clock boosting to enable operation at very low speed.

III. Measurement Results

This design was fabricated in 65nm CMOS and occupies an area of 0.08mm^2, including the reference and decoupling capacitors, as shown in Fig. 4. To characterize the chip, a trimming capacitor with a range of 1~30pF is used as the sensing capacitor. First, it is trimmed manually and measured with a GW INSTEK LCR-6100 meter for reference, and then it is connected to the chip to get the digital code. This process is repeated for different values of C_s, yielding the code versus C_s as shown in Fig. 5 (C_r = 5pF). As expected, higher ADC sensitivity increases the output code range, while lower ADC sensitivity supports a wider sensing range. Fig. 6 shows the measured output code with different C_r settings in double sided measurement and 4x ADC sensitivity mode. As discussed previously, the output code is inherently non-linear with C_s. A 3-point calibration is required to reconstruct the transfer function from C_s to the digital output, so that this non-linearity can be calibrated out. Fig. 7 shows the measured inaccuracy after calibration of each segment: the measured error is within ±8fF with a C_s range of 1.23~24.59pF. When C_r = 5pF, the rms resolution for single and double sided measurement at different ADC sensitivity settings are shown in Fig. 8. As expected, the double sided mode has about 3dB better resolution compared to the single sided mode. A higher ADC sensitivity has better resolution as it reduces both ADC quantization noise and kT/C noise. However, the resolution will eventually be limited by the thermal noise of the ADC's comparator which does not scale down. Thanks to the all-dynamic circuitry, the power scales proportionally with the speed (Fig. 9 top). The leakage power

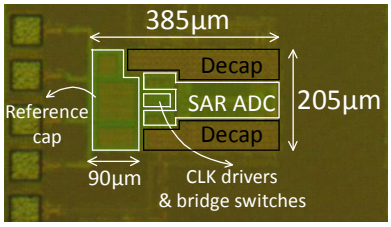

Fig. 4. Die photo in 65nm CMOS.

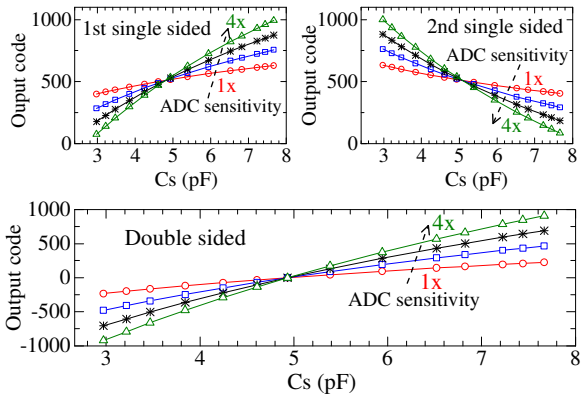

Fig. 5. Measured output code vs. C_s for various settings of ADC sensitivity when C_r = 5pF.

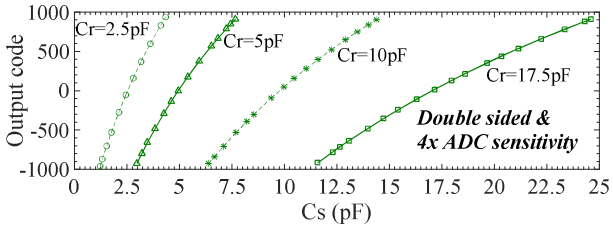

Fig. 6. Measured output code vs. C_s for various values of C_r.

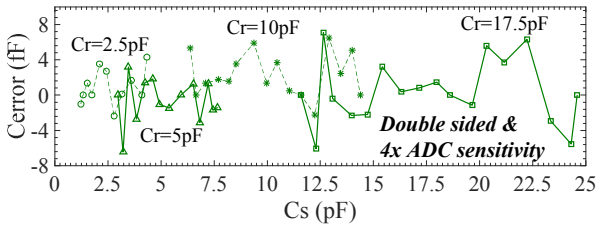

Fig. 7. Measured inaccuracy after 3-point calibration for various C_r.

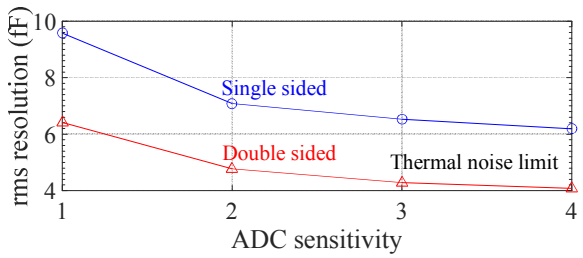

Fig. 8. rms resolution vs. ADC sensitivity when C_r = 5pF.

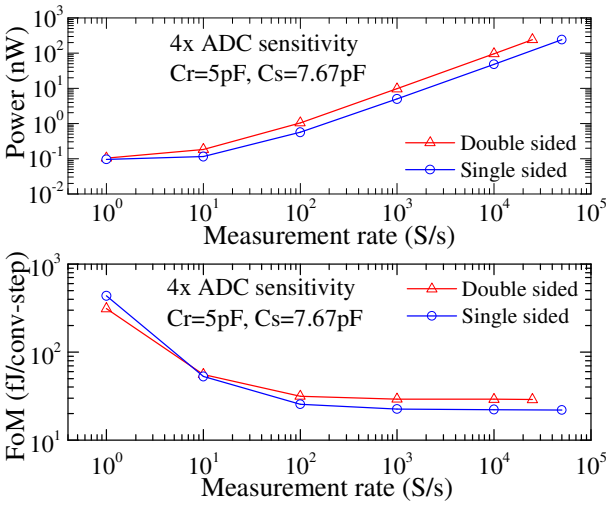

Fig. 9. Measured power vs. measurement rate (top), FoM vs. measurement rate (bottom) for C_r = 5pF and 4x ADC sensitivity.

is only 0.1nW, hence the FoM of this design can be well maintained even at a very low speed (Fig. 9 bottom).

The measured performance for different C_r settings at 4x ADC sensitivity mode is summarized in Table I. Similar SNR is obtained for different C_r settings. When C_r is small, the signal attenuation caused by C_p and C_{DAC} becomes more obvious, hence reducing the common mode voltage of the sampled input signal. The ADC's comparator with an NMOS input pair thus becomes slower, which leads to a lower maximum speed. The

TABLE I. MEASURED PERFORMANCE SUMMARY (4X ADC SENSITIVITY).

C_r (pF)	2.5		5		10		17.5		Combined	
Input range (pF)	1.23~4.33		2.97~7.67		6.38~14.38		11.58~24.59		1.23~24.59	
Single/double sided	single	double	single	double	single	double	single	double	single	double
Resolution (fF)	4.38	2.90	6.19	4.07	10.54	7.06	16.86	11.10	16.86	11.10
SNR [a] (dB)	47.97	51.55	48.58	52.22	48.57	52.05	48.72	52.35	53.80	57.43
Max. speed (kS/s)	20	10	50	25	100	50	100	50	100	50
Power [b] (nW)	73.8	74.7	240	242	695	694	1006	1004	1006	1004
E/conv. (pJ)	3.69	7.47	4.80	9.68	6.95	13.88	10.06	20.08	10.06	20.08
FoM [c] (fJ/conv-step)	18	24	22	29	32	42	45	59	25	33

[a] SNR = 20 log {Cap. range / ($2\sqrt{2}$ · Cap. resolution)} [c] FoM = (E/conv.)/$2^{(SNR-1.76)/6.02}$
[b] Power at max. speed, measured with largest C_s for each segment

power is measured with the largest C_s for each segment, which is the worst case. The ADC consumes about 1pJ/conversion according to post-layout simulations, and the rest is consumed by the bridge. A smaller C_r leads to lower energy per conversion, as the bridge consumption scales linear with the capacitance value. Therefore, better FoM is obtained for smaller C_r, yet all settings achieve a very competitive FoM from 18 to 59 fJ/conv-step.

Table II summarizes speed and power scalability of this design (C_r = 17.5pF, 4x ADC sensitivity mode). The speed of this design can scale over 5 orders of magnitude, and 4 orders of magnitude scalability is achieved in power. Both are well beyond the prior-art, making this design able to deal with different sensors and applications easily and efficiently.

To verify this design with a real capacitive sensor, a Murata MEMS pressure sensor is bonded to the chip and characterized in a pressure chamber. An NXP MPXH6400A pressure sensor is placed close to the chip as a reference. C_r is set to 10pF, and 4x ADC sensitivity is used. Fig. 10 shows that the measured result by this chip after calibration can very well follow the results from the commercial reference, while only 0.8nW power is consumed at the single sided mode with a speed of 100S/s.

TABLE II. SPEED AND POWER SCALABILITY COMPARISON.

	[1] [a]	[5] [a]	[6]	This work [b]	
				Single	Double
Speed range (S/s)	15.6k~62.5k	0.5k~6.3k	30~100000	1~100000	1~50000
Scaling factor [c]	4	12.6	3333	100k	50k
Power range (W)	1.81µ~7.25µ	16µ~42µ	2.8n~8820n	0.1n~1006n	0.1n~1004n
Scaling factor [c]	4	2.625	3150	10k	10k

[a] Estimated numbers [b] Measured results with C_r = 17.5pF & 4x ADC sensitivity
[c] Scaling factor = max. value / min. value

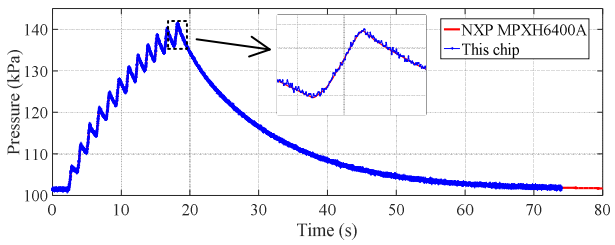

Fig. 10. Pressure measurement and comparison to a commerical sensor.

TABLE III. COMPARISON WITH PRIOR ART.

	[1]	[2]	[3]	[4]	[6]	This work [a]	
Method	SAR	SAR + VCO	Dual Slope	SAR	SAR	SAR	
Technology	180nm	40nm	180nm	180nm	180nm	65nm	
Cap. range (pF)	0~12.66	0~5	5.3~30.7	2.5~75.3	N/A	2.97~7.67	
Resolution (fF)	1.1	1.1	8.7 [b]	6	N/A	Single	Double
						6.19	4.07
SNR (dB)	72.19	64.2	44.2 [b]	72.65	N/A	48.58	52.22
Speed (S/s)	62.5k	1M	156.25	250	30~100000	1~50000	1~25000
Power (nW)	7250	75000	110	160	2.8~8820	0.1~240	0.1~242
E/conv. (pJ)	116	75	704	640	88 [c]	4.80 [c]	9.68 [c]
FoM (fJ/conv-step)	35	55	5300 [b]	183	290 [d]	22 [c]	29 [c]

[a] Measured results with C_r = 5pF & 4x ADC sensitivity [b] Calculated with one subrange
[c] @ max. speed [d] ENOB-based FoM definition in this work

IV. CONCLUSION

Table III compares the performance of this work (C_r = 5pF, 4x ADC sensitivity mode) with prior-art. An SNR of 48.58/52.22dB is obtained at single/double sided mode with a maximum speed of 50/25kS/s. A lowest reported absolute power of 0.1nW is achieved at 1S/s, which is >20x smaller than prior art. A reported lowest FoM of 22/29fJ/conv-step is also achieved (at max. speed) with single and double sided mode respectively. Note that with smaller C_r, the FoM further improves down to 18fJ/conv-step. Thanks to the all-dynamic architecture, the power scales proportionally with the speed up to 4 orders of magnitude. Overall, this design combines state-of-the-art power efficiency with the lowest power and highest versatility, such that a wide variety of sensor types and IoT applications can be supported optimally.

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